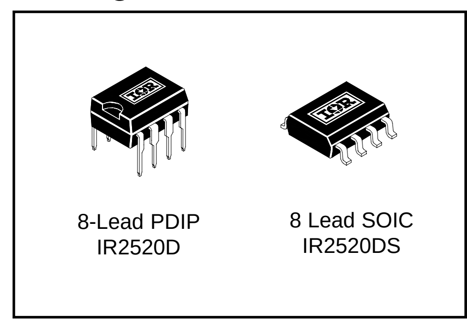
IR2520D(S)

ADAPTIVE BALLAST CONTROL IC

Features

- 600V Half Bridge Driver
- Integrated Bootstrap Diode
- Adaptive zero-voltage switching (ZVS)
- Internal Crest Factor Over-Current Protection
- 0 to 5VDC Voltage Controlled Oscillator
- Programmable minimum frequency
- Micropower Startup Current (150uA)
- Internal 15.6V zener clamp on Vcc
- Small DIP8/SO8 Package

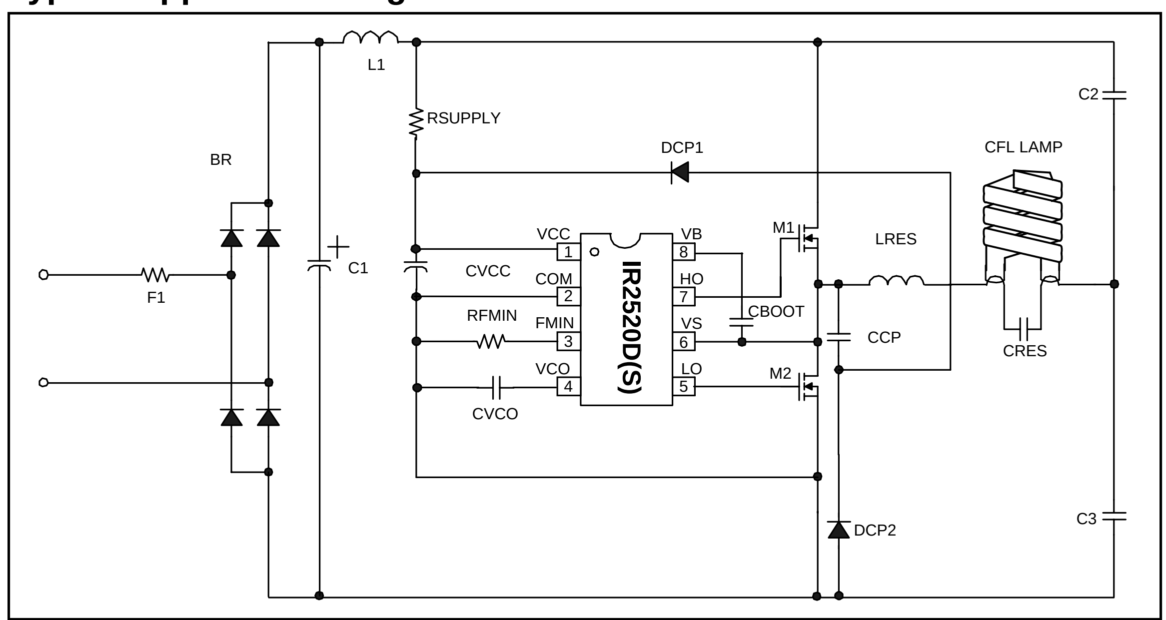
Packages



Description

The IR2520D(S) is a complete adaptive ballast controller and 600V half-bridge driver integrated into a single IC for fluorescent lighting applications. The IC includes adaptive zero-voltage switching (ZVS), internal crest factor over-current protection, as well as an integrated bootstrap diode. The heart of this IC is a voltage controlled oscillator with externally programmable minimum frequency. All of the necessary ballast features are integrated in a small 8-pin DIP or SOIC package.

Typical Application Diagram



Please note that this data sheet contains advance information which could change before product is released to production.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
I_{OMAX}	Maximum allowable output current (HO,LO) due to external power transistor miller effect		-500	500	mA
I_{VCO}	Voltage controlled oscillator input current (Note 1)		-5	+ 5	mA
I_{CC}	Supply current (Note 2)		-20	20	mA
dV_S/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ $T_A \le +25°C$	8-Lead PDIP	—	1	W
	$PD=(T_{JMAX}-T_A)Rth_{JA}$	8-Lead SOIC	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead PDIP	—	125	°C/W
		8-Lead SOIC	—	200	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: This IC contains a zener clamp structure between the chip VCO and COM, which has a nominal breakdown voltage of 6V. Please note that this pin should not be driven by a DC, low impedance power source greater than 6V.

Note 2: This IC contains a zener clamp structure between the chip VCC and COM, which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-1	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	Note 3	10	mA
R_{FMIN}	Minimum frequency setting resistance	10	100	kΩ
V_{VCO}	VCO pin voltage	0	5	V
T_J	Junction temperature	-25	125	°C

Note 3: Enough current should be supplied into the VCC pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage, VCLAMP.

Electrical Characteristics

$V_{CC} = V_{BS} = V_{BIAS}$ = 14V +/- 0.25V, C_{LO}=C_{HO}=1000pF, R_{FMIN} = 82K and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	11.5	12.7	13.9	V	V_{CC} rising from OV
V_{CCUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	9.0	10	11.0		
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	—	2.7	—		
I_{QCCUV}	UVLO quiescent current	40	50	70	µA	V_{CC} = 10V
I_{QCCFLT}	Fault mode quiescent current	—	180	—		
I_{CCHF}	V_{CC} supply current f=85KHz	3.0	4.0	6.0	mA	V_{VCO}=0V
I_{CCLF}	V_{CC} supply current f=35KHz	1.0	2.0	3.0		V_{VCO}=6V
V_{CLAMP}	V_{CC} Zener clamp voltage	14.5	15.6	16.5	V	I_{CC} = 10mA
Floating Supply Characteristics						
I_{QBS0}	Quiescent V_{BS} supply current	60	90	110	µA	V_{CC}=10V, V_{BS}=14V
I_{QBSUV}	Quiescent V_{BS} supply current	10	20	30		V_{CC}=10V, V_{BS}=7V
I_{LK}	Offset supply leakage current	—	—	50		V_B = V_S = 600V
Oscillator I/O Characteristics						
$f_{(min)}$	Minimum oscillator frequency (Note 4)	—	35	—	kHz	V_{VCO}=6V
$f_{(max)}$	Maximum oscillator frequency (Note 4)	—	85	—		V_{VCO}=0V
D	Oscillator duty cycle	—	50	—	%	
DT_{LO}	LO output deadtime	1.5	1.8	2.1	µS	
DT_{HO}	HO output deadtime	1.8	2.1	2.4		
I_{VCOQS}	I_{VCO} quick start	20	40	60	µA	V_{VCO}=0V
I_{VCOFS}	I_{VCO} frequency sweep	0.9	1.1	1.3		V_{VCO}=2V
Gate Driver Output Characteristics						
$V_{LO=LOW}$	V_{LO} -V_{COM} difference between LO output voltage and COM when LO is low	—	0	100	mV	V_{VCO}=6V
$V_{HO=LOW}$	V_{HO} -V_S difference between HO output voltage and V_S when HO is low	—	0	100		V_{VCO}=6V
$V_{LO=HIGH}$	V_{CC} -V_S difference between VCC and LO output voltage when LO is high	—	0	100		V_{VCO}=6V
$V_{HO=HIGH}$	V_B -V_{HO} difference between V_B and HO output voltage when HO is high	—	0	100		V_{VCO}=6V
T_{RISE}	Turn on rise time	—	—	200	nS	
T_{FALL}	Turn off fall time	—	—	100		

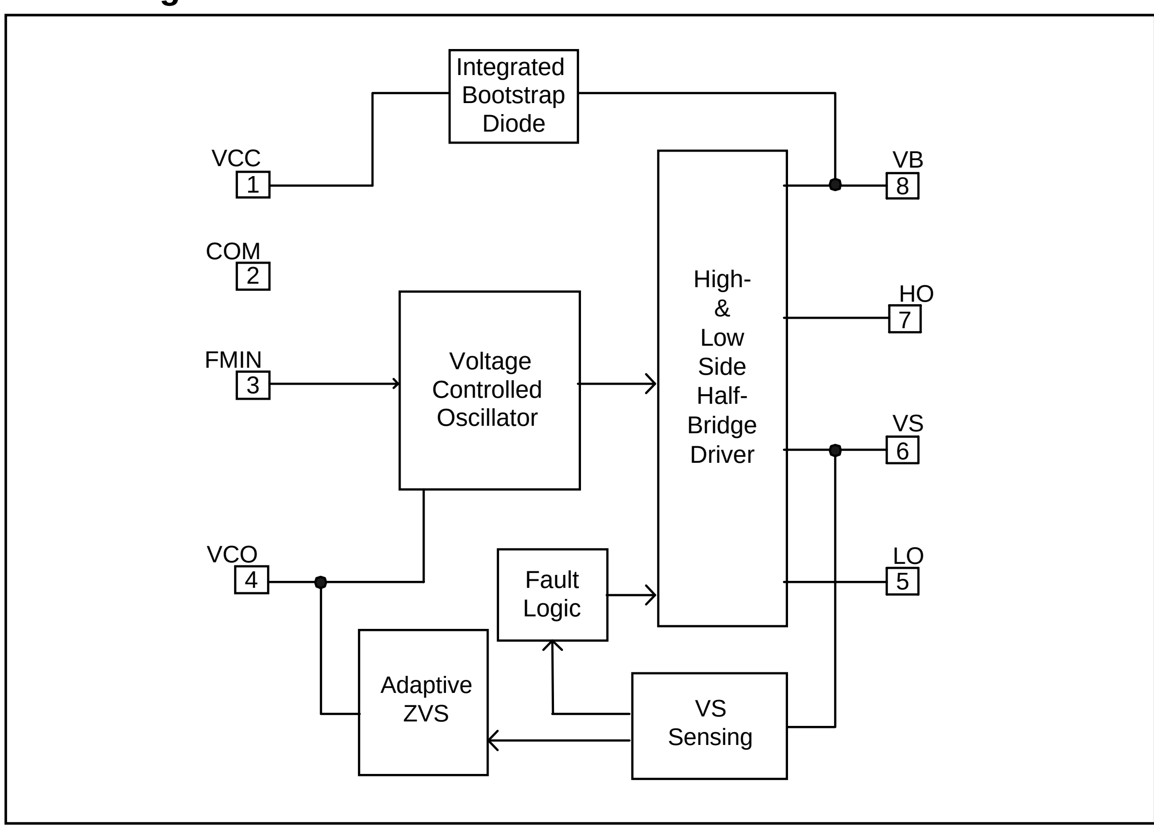
Note 4: Frequency shown is nominal for R_{FMIN}=82K. Frequency can be programmed higher or lower depending on the value of R_{FMIN}.

Electrical Characteristics

$V_{CC} = V_{BS} = V_{BIAS}$ = 14V +/- 0.25V, C_{LO}=C_{HO}=1000pF, R_{FMIN} = 82K and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Protection Characteristics						
CSCF	Crest factor peak-to-average fault factor	—	5.0	—	N/A	
V_{VCOSD}	V_{VCO} shutdown voltage	—	0.85	—	V	
Minimum Frequency Setting Characteristics						
V_{FMIN}	FMIN lead voltage during normal operation	—	5.1	—	V	
$V_{FMINFLT}$	FMIN lead voltage during fault mode	—	0.0	—	V	

Block Diagram



Lead Definitions

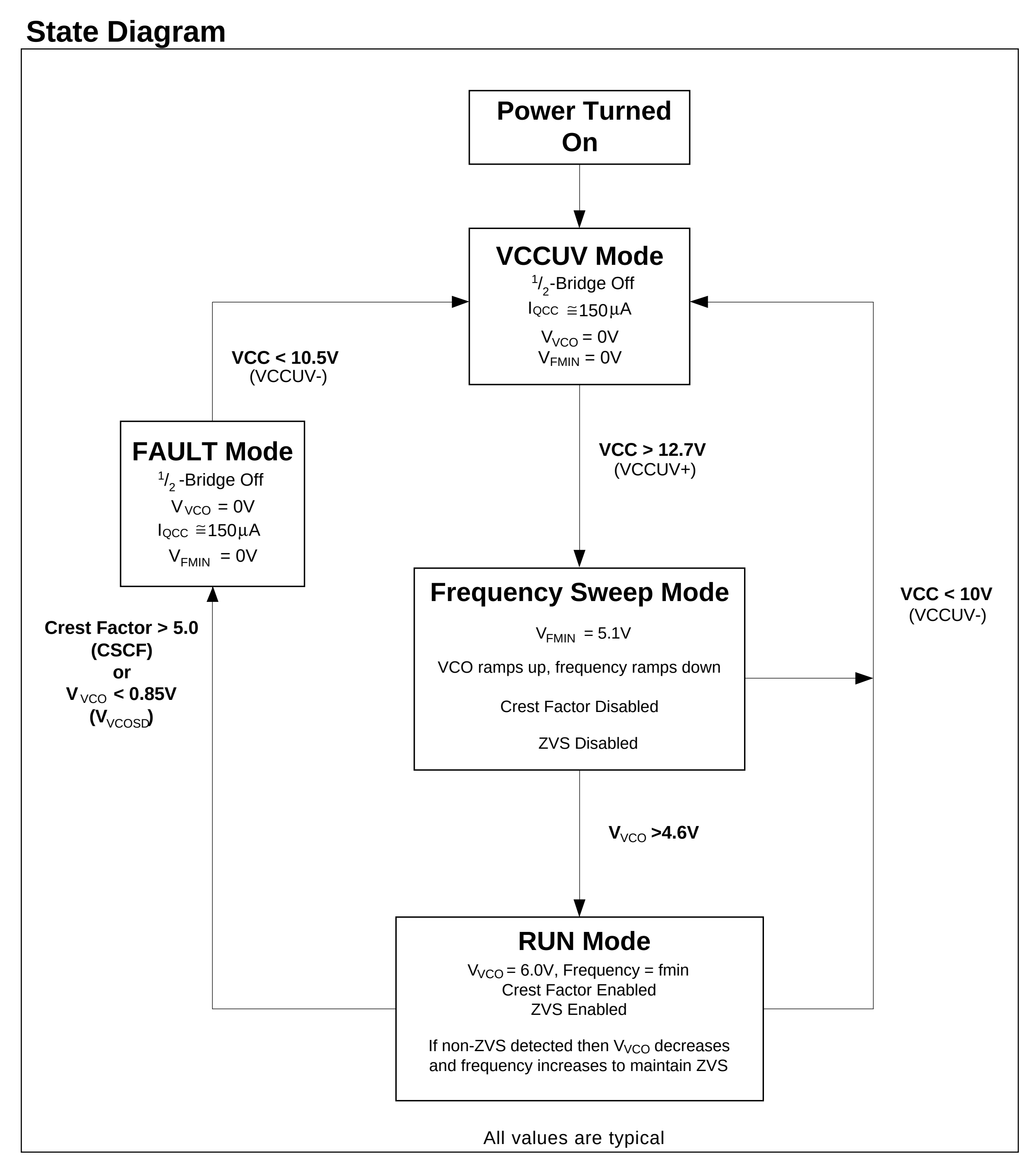
Symbol	Description
V_{CC}	Supply voltage
COM	IC power and signal ground
FMIN	Minimum frequency setting
VCO	Voltage controlled oscillator input
LO	Low-side gate driver output
V_S	High-side floating return
HO	High-side gate driver output
VB	High-side gate driver floating supply

Lead Assignments

Pin	Name	Pin	Name
1	VCC	8	VB
2	COM	7	HO
3	FMIN	6	VS
4	VCO	5	LO

IR2520D(S)

State Diagram



Functional Description

Under-voltage Lock-Out Mode

The under-voltage lockout mode (UVLO) is defined as the state the IR2520D is in when VCC is below the turn-on threshold of the IC. The IR2520D under voltage lock-out is designed to maintain an ultra low supply current (<200uA), and to guarantee that the IR2520D is fully functional before the high and low side output drivers are activated.

The start-up capacitor, C_{VCC}, is charged by current through supply resistor, R_{SUPPLY}, minus the start-up current drawn by the IR2520D. This resistor is chosen to provide sufficient current to supply the IR2520D from the DC bus. C_{VCC} should be large enough to hold the voltage at Vcc above the UVLO threshold for one half cycle of the line voltage as it will only be charged at the peak. Once the capacitor voltage on V_{CC} reaches the start-up threshold, the IR2520D turns on and then HO and LO start oscillating.

An internal bootstrap diode between Vcc and VB and external supply capacitor, C_{BOOT}, determine the supply voltage for the high side driver circuitry. An external charge pump circuit consisting of a capacitor, C_{CP}, and two diodes, D_{CP1} and D_{CP2}, supplies the voltage for the low side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. LO may oscillate several times until VB-VS exceeds UVBS+ (9 Volts) and the high-side driver is enabled.

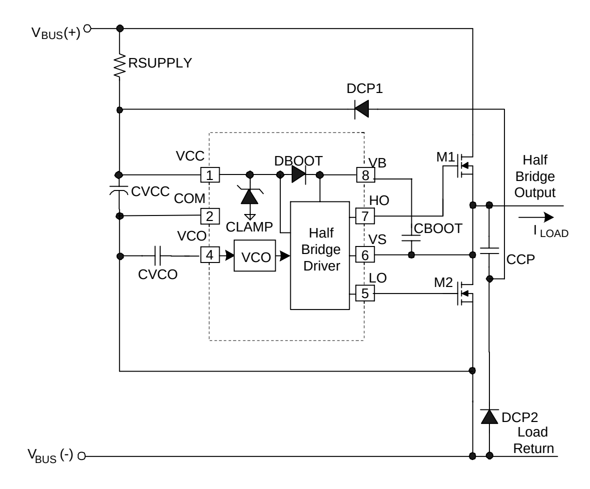


Figure 1, Start-up circuitry

During UVLO mode, the high and low-side driver outputs, HO and LO, are both low and pin VCO is pulled down to COM for resetting the starting frequency to the maximum.

Frequency Sweep Mode

When VCC exceeds UVLO+ threshold, the IR2520D enters frequency sweep mode. An internal current source charges the external capacitor on pin VCO, C_{VCO}, and the voltage on pin VCO starts ramping up linearly. The frequency ramps down towards the resonance frequency of the high-Q ballast output stage causing the lamp voltage and load current to increase. The voltage on pin VCO continues to increase and the frequency keeps decreasing until the lamp ignites.If the lamp ignites successfully, the voltage on pin VCO continues to increase until it internally limits at 6V. The frequency stops decreasing and stays at the minimum frequency as programmed by an external resistor, RFMIN, on pin FMIN. The minimum frequency should be set below the high-Q resonance frequency of the ballast output stage to ensure that the frequency ramps through resonance for lamp ignition. The desired preheat time can be set by adjusting the slope of the VCO ramp with the external capacitor, C_{VCO}.

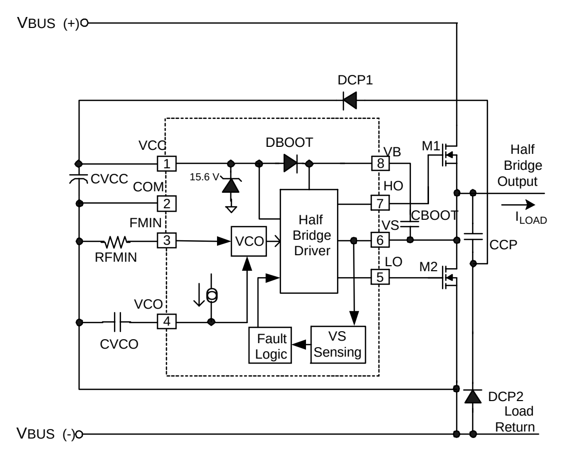


Figure 2, Frequency sweep circuitry

Run Mode

The frequency decreases during the frequency sweep mode until the lamp ignites and the ballast output stage becomes a low-Q RCL circuit. The frequency then deceases further until the VCO pin voltage limits at 6V and the minimum frequency is reached. The resonant inductor, resonant capacitor, DC bus voltage and minimum frequency determine the running lamp power. The IC stays at this minimum frequency unless non-zero-voltage switching (non-ZVS) is detected at the VS pin. If the VS voltage has not slewed entirely to COM during the deadtime such that there is voltage across the external low-side switch before LO turns-on, then the system is operating too close to resonance and destructive non-ZVS capacitive mode switching occurs. To correct for this, a pulse of current is sinked from the VCO pin to discharge the external capacitor, C_{VCO}, causing the frequency to increase slightly. The VCO capacitor then charges up during the rest of the cycle slowly due to an internal current source. The frequency is therefore trying to decrease towards resonance by charging the VCO capacitor and the adaptive ZVS circuit "nudges" the frequency back up slightly above resonance when non-ZVS occurs. The circuit then remains in this closed-loop adaptive ZVS mode during running and maintains ZVS operation with changing line conditions, component tolerance variations and lamp/ load variations. The 600V fabrication process used in the development of this IC allows for the VS pin to be accurately measured with an internal high-voltage MOSFET for zero volts during the non-overlapping deadtime, while withstanding the high DC bus voltage during other portions of the switching cycle when the high-side MOSFET is turned on and VS is at the DC bus potential.

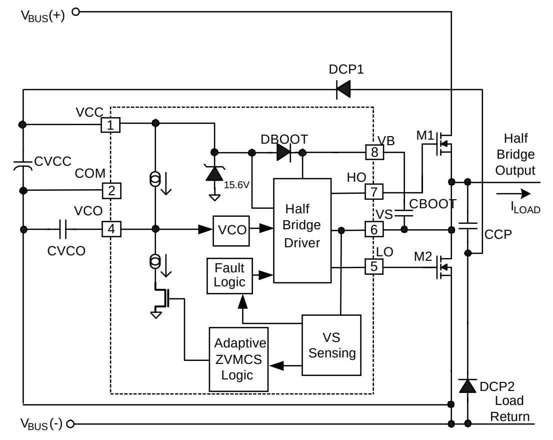


Figure 3, ZVS circuitry

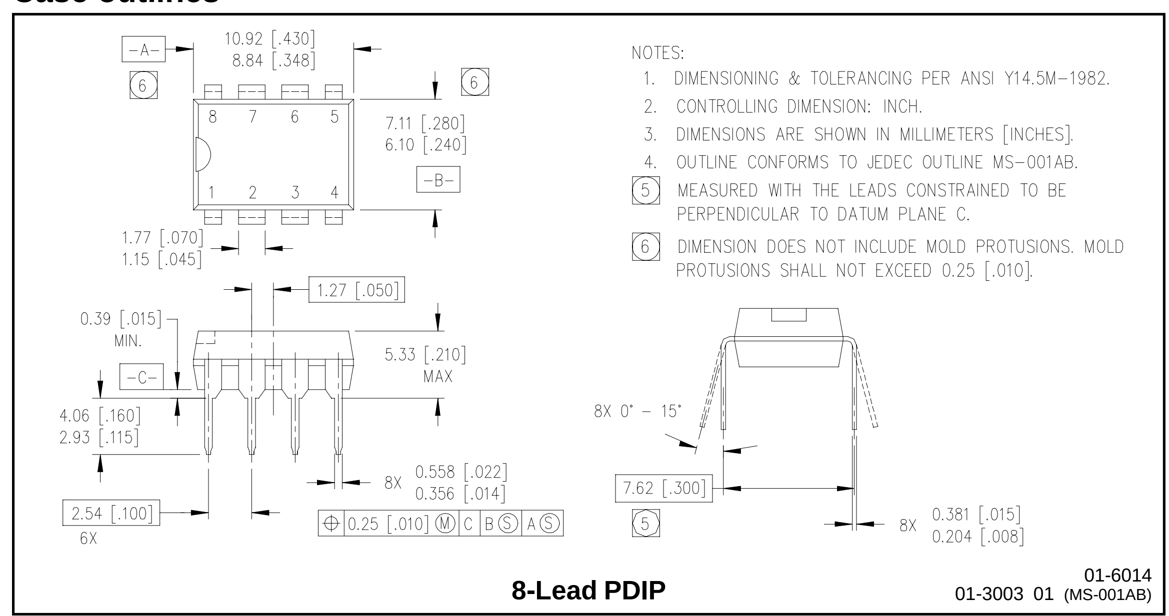
Fault Mode

Should a lamp non-strike condition occur where the filaments are intact but the lamp does not ignite, the lamp voltage and output stage current will increase during the ignition ramp until the resonant inductor saturates or capacitive mode switching occurs. To detect this, the IC performs a measurement of the VS pin during the on-time of the LO pin. The voltage at the VS pin during the on-time of pin LO is determined by the current flowing through the on-resistance (RDSon) of the external low-side MOSFET. The RDSon of the external low-side MOSFET therefore serves as the current-sensing resistor and VS serves as the current sensing pin on the IC. Sensing the half-bridge current in this way eliminates the need for an external current-sensing resistor and an additional current-sensing pin on the IC. An internal high-voltage MOSFET is turned on when VS is low (when the external low-side MOSFET is "on") for performing the current sensing, and is turned off during the rest of the switching cycle for withstanding the high-voltage when VS is equal to the DC bus voltage (when the external high-side MOSFET is "on"). Since the RDSon has a positive temperature coefficient, the IC performs an internal crest factor measurement for detecting excessive dangerous currents or inductor saturation which can occur during a lamp non-strike fault condition. Performing the crest factor measurement provides a relative current measurement which cancels temperature and/or tolerance variations of the RDSon of the external low-side half-bridge MOSFET. Should the peak current during the on-time of LO exceed a threshold of 5.0 times the average current, the IC will enter Fault Mode and both gate driver outputs will be latched "low". To reset the IC back to frequency sweep mode VCC must be recycled below and above the internal UVLO thresholds.

Should an open filament lamp fault occur, hard-switching will occur at the half-bridge. The non-ZVS circuit will detect this and decrease the VCO voltage each cycle to increase the frequency for maintaining ZVS. Should the VCO voltage decrease below 1V, the IC will enter Fault Mode and both gate driver outputs will be latched "low". To reset the IC back to frequency sweep mode VCC must be recycled below and above the internal UVLO thresholds

Both the 1V latched VCO threshold and the crest factor protection are enabled when V_{VCO} exceeds 4.6V for the first time during the frequency sweep mode (see State Diagram). This prevents false triggering of the Fault Mode during normal preheat or normal lamp ignition.

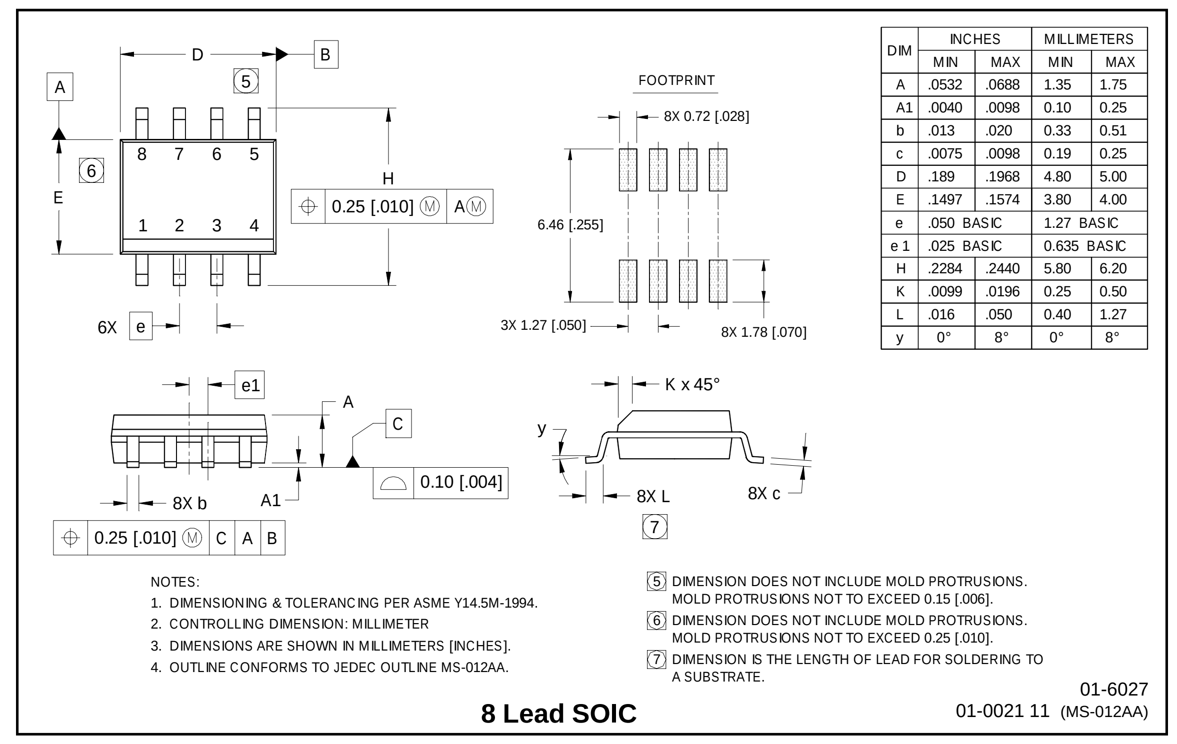
Case outlines



8-Lead PDIP

IR2520D

ADVANCE DATA



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

8 Lead SOIC

IR2520DS

International IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 2/6/2004